



Single Supply / Low Power / 256-tap / SPI bus

## X9261

### Dual Digitally-Controlled (XDCP™) Potentiometers

#### FEATURES

- Dual—Two Separate Potentiometers
- 256 resistor taps/pot—0.4% resolution
- SPI Serial Interface for write, read, and transfer operations of the potentiometer single supply device
- Wiper Resistance, 100Ω typical @  $V_{CC} = 5V$
- 4 Nonvolatile Data Registers for Each Potentiometer
- Nonvolatile Storage of Multiple Wiper Positions
- Power On Recall Loads Saved Wiper Position on Power Up.
- Standby Current < 5μA Max
- 50KΩ, 100KΩ versions of End to End Resistance
- 100 yr. Data Retention
- Endurance: 100,000 Data Changes per Bit per Register
- 24-Lead SOIC, 24-Lead TSSOP, 16-Lead CSP (Chip Scale Package)
- Low Power CMOS
- Power Supply  $V_{CC} = 2.7V$  to 5.5V

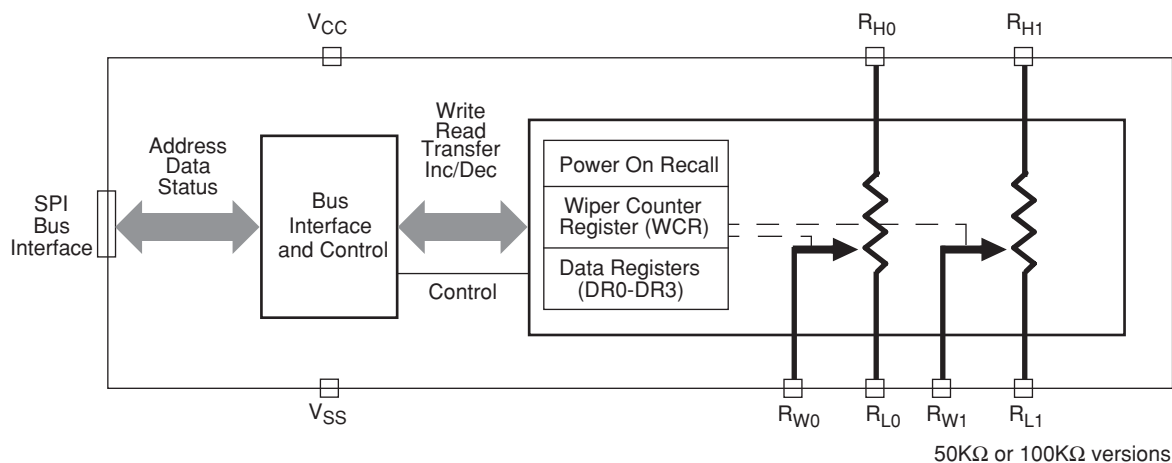
#### DESCRIPTION

The X9261 integrates 2 digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

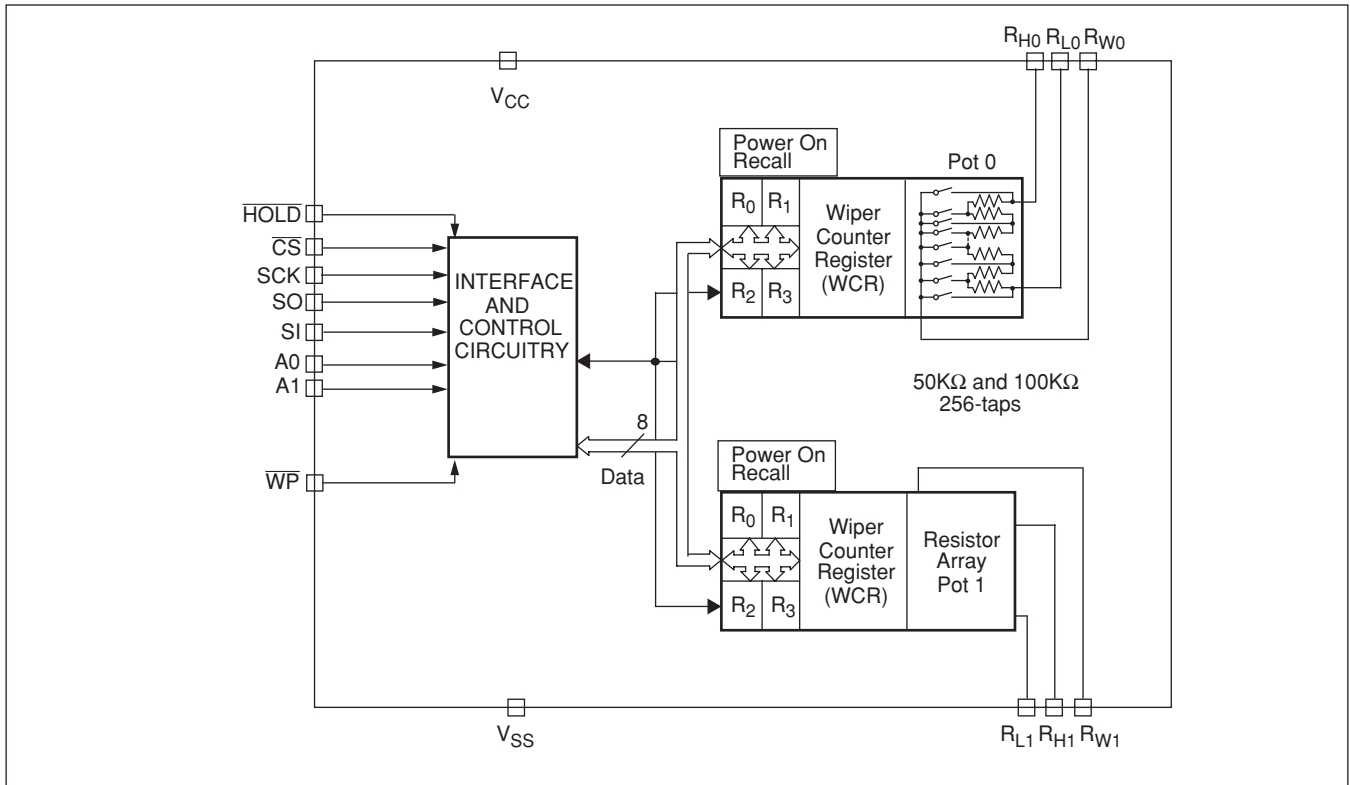
The digital controlled potentiometer is implemented using 255 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Powerup recalls the contents of the default Data Register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

#### FUNCTIONAL DIAGRAM



## DETAILED FUNCTIONAL DIAGRAM



### CIRCUIT LEVEL APPLICATIONS

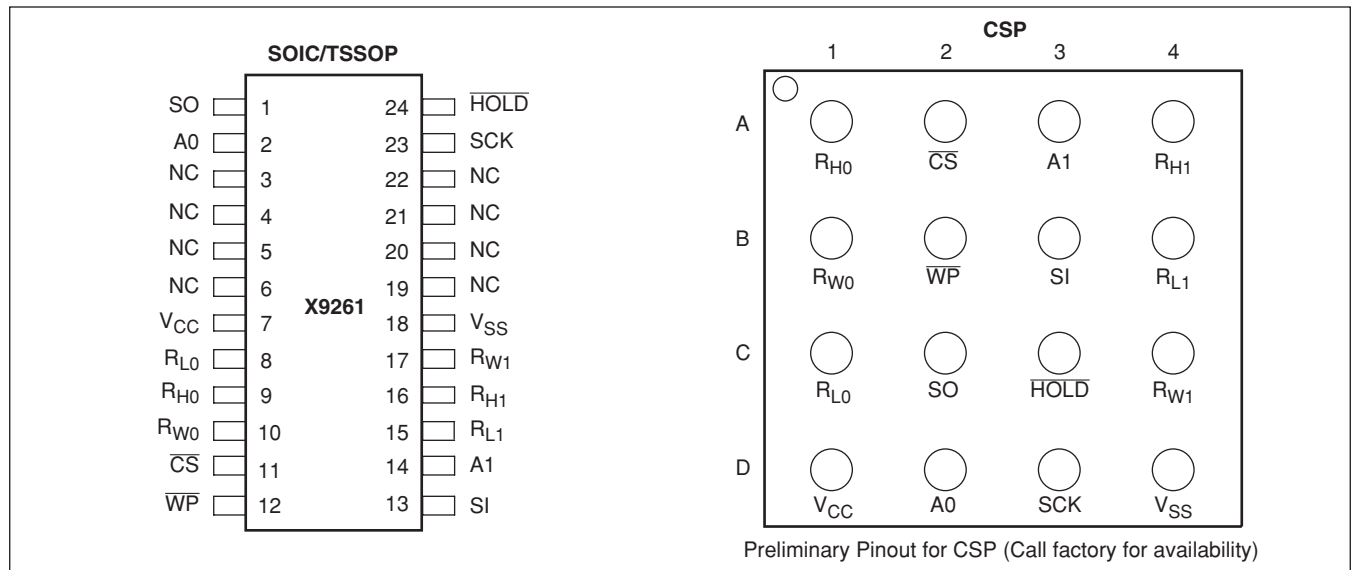
- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

### SYSTEM LEVEL APPLICATIONS

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

# X9261

## PIN CONFIGURATION



## PIN ASSIGNMENTS

Pin (SOIC/TSSOP)	Pin CSP	Symbol	Function
1	C2	SO	Serial Data Output for SPI bus
2	D2	A0	Device Address for SPI bus.
3	N/A	NC	No Connect.
4	N/A	NC	No Connect.
5	N/A	NC	No Connect.
6	N/A	NC	No Connect.
7	D1	V <sub>CC</sub>	System Supply Voltage
8	C1	R <sub>L0</sub>	Low Terminal for Potentiometer 0.
9	A1	R <sub>H0</sub>	High Terminal for Potentiometer 0.
10	B1	R <sub>W0</sub>	Wiper Terminal for Potentiometer 0.
11	A2	CS	Device Address for SPI bus.
12	B2	WP	Hardware Write Protect
13	B3	SI	Serial Data Input for SPI bus
14	A3	A1	Device Address for SPI bus.
15	B4	R <sub>L1</sub>	Low Terminal for Potentiometer 1.
16	A4	R <sub>H1</sub>	High Terminal for Potentiometer 1.
17	C4	R <sub>W1</sub>	Wiper Terminal for Potentiometer 1.
18	D4	V <sub>SS</sub>	System Ground
19	N/A	NC	No Connect
20	N/A	NC	No Connect
21	N/A	NC	No Connect
22	N/A	NC	No Connect
23	D3	SCK	Serial Clock for SPI bus
24	C3	HOLD	Device select. Pause the SPI serial bus.

# X9261

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## PIN DESCRIPTIONS

### Bus Interface Pins

#### SERIAL OUTPUT (SO)

SO is a serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

#### SERIAL INPUT

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input on this pin. Data is latched by the rising edge of the serial clock.

#### SERIAL CLOCK (SCK)

The SCK input is used to clock data into and out of the X9261.

#### HOLD ( $\overline{\text{HOLD}}$ )

$\overline{\text{HOLD}}$  is used in conjunction with the  $\overline{\text{CS}}$  pin to select the device. Once the part is selected and a serial sequence is underway,  $\overline{\text{HOLD}}$  may be used to pause the serial communication with the controller without resetting the serial sequence. To pause,  $\overline{\text{HOLD}}$  must be brought LOW while SCK is LOW. To resume communication,  $\overline{\text{HOLD}}$  is brought HIGH, again while SCK is LOW. If the pause feature is not used,  $\overline{\text{HOLD}}$  should be held HIGH at all times.

#### DEVICE ADDRESS (A1–A0)

The address inputs are used to set the 4-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9261.

#### CHIP SELECT ( $\overline{\text{CS}}$ )

When  $\overline{\text{CS}}$  is HIGH, the X9261 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state.  $\overline{\text{CS}}$  LOW enables the X9261, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on  $\overline{\text{CS}}$  is required prior to the start of any operation.

### Potentiometer Pins

#### R<sub>H</sub>, R<sub>L</sub>

The R<sub>H</sub> and R<sub>L</sub> pins are equivalent to the terminal connections on a mechanical potentiometer. Since there are 2 potentiometers, there are 2 sets of R<sub>H</sub> and R<sub>L</sub> such that R<sub>H0</sub> and R<sub>L0</sub> are the terminals of POT 0 and so on.

#### R<sub>W</sub>

The wiper pin are equivalent to the wiper terminal of a mechanical potentiometer. Since there are 2 potentiometers, there are 2 sets of R<sub>W</sub> such that R<sub>W0</sub> is the terminals of POT 0 and so on.

### Supply Pins

#### SYSTEM SUPPLY VOLTAGE (V<sub>CC</sub>) AND SUPPLY GROUND (V<sub>SS</sub>)

The V<sub>CC</sub> pin is the system supply voltage. The V<sub>SS</sub> pin is the system ground.

### Other Pins

#### No CONNECT

No connect pins should be left floating. This pins are used for Xicor manufacturing and testing purposes.

#### HARDWARE WRITE PROTECT INPUT ( $\overline{\text{WP}}$ )

The  $\overline{\text{WP}}$  pin when LOW prevents nonvolatile writes to the Data Registers.

# X9261

## PRINCIPLES OF OPERATION

### Serial Interface

The X9261 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK.  $\overline{CS}$  must be LOW and the  $\overline{HOLD}$  and  $\overline{WP}$  pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

### Array Description

The X9261 is comprised of a resistor array (see Figure 1). The array contains the equivalent of 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer ( $R_H$  and  $R_L$  inputs).

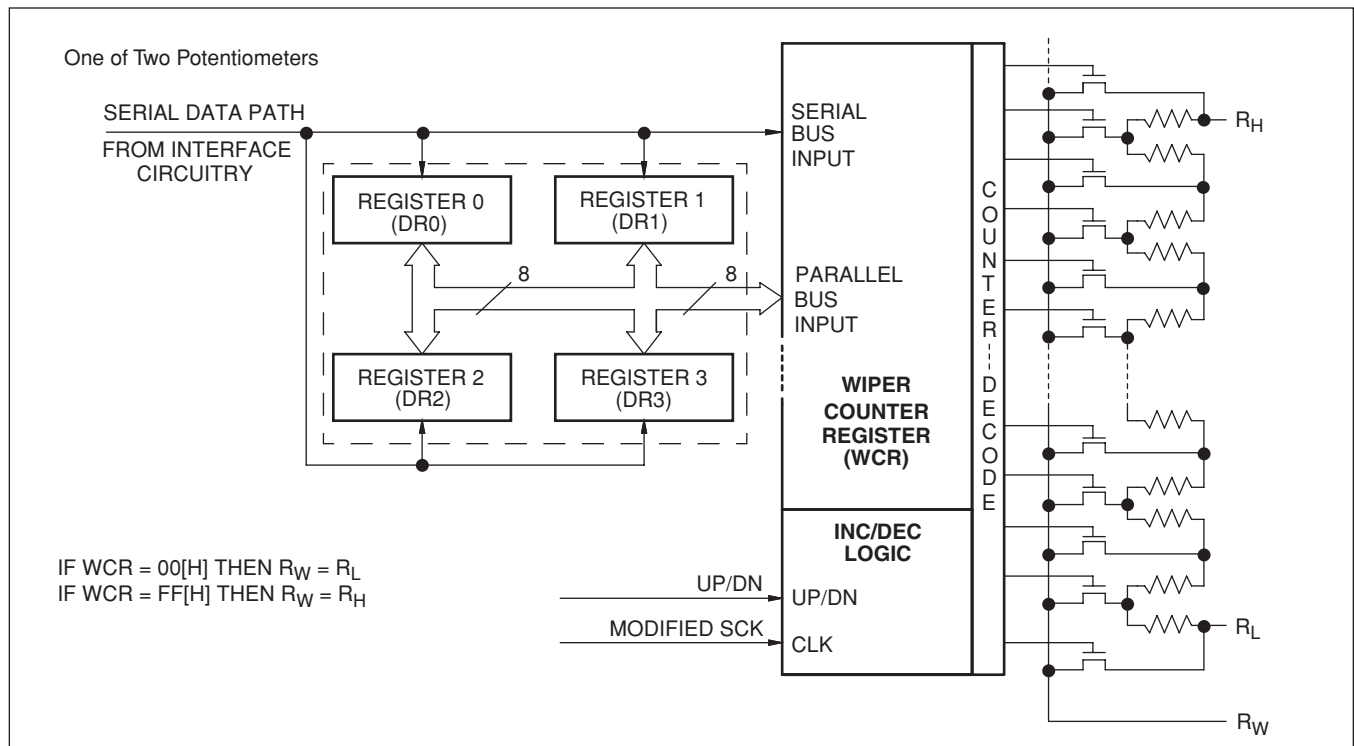
At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper ( $R_W$ ) output. Within each individual array only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The 8-bits of the WCR (WCR[7:0]) are decoded to select, and enable, one of 256 switches (see Table 1).

### Power Up and Down Requirements.

There are no restrictions on the power-up or power-down conditions of  $V_{CC}$  and the voltages applied to the potentiometer pins provided that  $V_{CC}$  is always more positive than or equal to  $V_H$ ,  $V_L$ , and  $V_W$ , i.e.,  $V_{CC}$ ,  $V_H$ ,  $V_L$ ,  $V_W$ . The  $V_{CC}$  ramp rate specification is always in effect.

Figure 1. Detailed Potentiometer Block Diagram



## DEVICE DESCRIPTION

### Wiper Counter Register (WCR)

The X9261 contains two Wiper Counter Registers, one for each DCP potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction (see Instruction section for more details). Finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9261 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR0 value into the WCR.

### Data Registers (DR)

Each potentiometer has four 8-bit nonvolatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bits [7:0] are used to store one of the 256 wiper positions or data (0~255).

### Status Register (SR)

This 1-bit Status Register is used to store the system status.

WIP: Write In Progress status bit, read only.

- When WIP=1, indicates that high-voltage write cycle is in progress.
- When WIP=0, indicates that no high-voltage write cycle is in progress.

**Table 1. Wiper Counter Register, WCR (8-bit), WCR[7:0]:** Used to store the current wiper position (Volatile, V).

WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
V	V	V	V	V	V	V	V
(MSB)							(LSB)

**Table 2. Data Register, DR (8-bit), Bit [7:0]:** Used to store wiper positions or data (Nonvolatile, NV).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NV	NV	NV	NV	NV	NV	NV	NV
MSB							LSB

# X9261

## DEVICE DESCRIPTION

### Instructions

#### IDENTIFICATION BYTE ( ID AND A )

The first byte sent to the X9261 from the host, following a  $\overline{CS}$  going HIGH to LOW, is called the Identification Byte. The most significant four bits of the slave address are a device type identifier. The ID[3:0] bits is the device id for the X9261; this is fixed as 0101[B] (refer to Table 3).

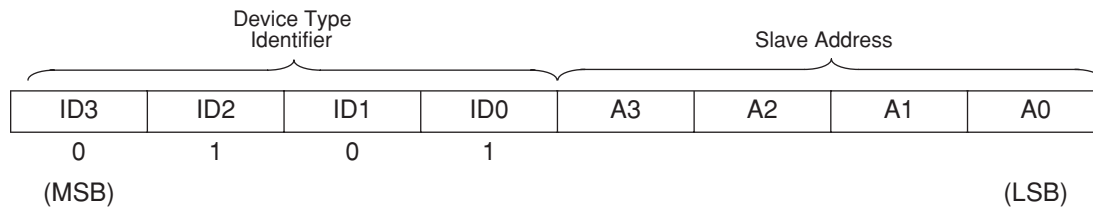
The AD[3:0] bits in the ID byte is the internal slave address. The physical device address is defined by the state of the A3-A0 input pins. The slave address is externally specified by the user. The X9261 compares the serial data stream with the address input state; a

successful compare of both address bits is required for the X9261 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A3-A0 inputs can be actively driven by CMOS input signals or tied to  $V_{CC}$  or  $V_{SS}$ .

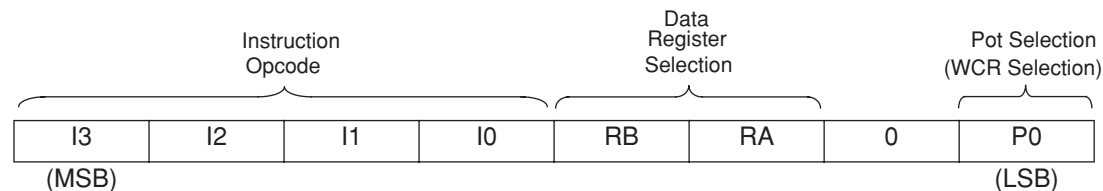
#### INSTRUCTION BYTE ( I[3:0] )

The next byte sent to the X9261 contains the instruction and register pointer information. The three most significant bits are used provide the instruction opcode (I[3:0]). The RB and RA bits point to one of the four Data Registers of each associated XDCCP. The least significant bit points to one of two Wiper Counter Registers or Pots. The format is shown below in Table 4.

**Table 3. Identification Byte Format**



**Table 4. Instruction Byte Format**



### Register Selection

Register Selected	RB	RA
DR0	0	0
DR1	0	1
DR2	1	0
DR3	1	1

## DEVICE DESCRIPTION

### Instructions

Four of the ten instructions are three bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the selected potentiometer,
  - **Write Wiper Counter Register** – change current wiper position of the selected potentiometer,
  - **Read Data Register** – read the contents of the selected Data Register;
  - **Write Data Register** – write a new value to the selected Data Register.
- **Read Status** - This command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

The basic sequence of the three byte instructions is illustrated in Figure 3. These three-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by  $t_{WRL}$ . A transfer from the WCR (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of  $t_{WR}$  to complete. The transfer can occur between one of the two potentiometers and one of its associated registers; or it may occur globally, where the transfer occurs between all potentiometers and one associated register. The Read Status Register instruction is the only unique format (see Figure 5).

Four instructions require a two-byte sequence to complete. These instructions transfer data between the host and the X9261; either between the host and one

of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.
- **Global XFR Data Register to Wiper Counter Register** – This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.
- **Global XFR Wiper Counter Register to Data Register** – This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

## INCREMENT/DECREMENT COMMAND

The final command is Increment/Decrement (see Figures 6 and 7). The Increment/Decrement command is different from the other commands. Once the command is issued and the X9261 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse ( $t_{HIGH}$ ) while SI is HIGH, the selected wiper will move one resistor segment towards the  $R_H$  terminal. Similarly, for each SCL clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the  $R_L$  terminal. A detailed illustration of the sequence and timing for this operation are shown. See Instruction format for more details.



Figure 2. Two-Byte Instruction Sequence

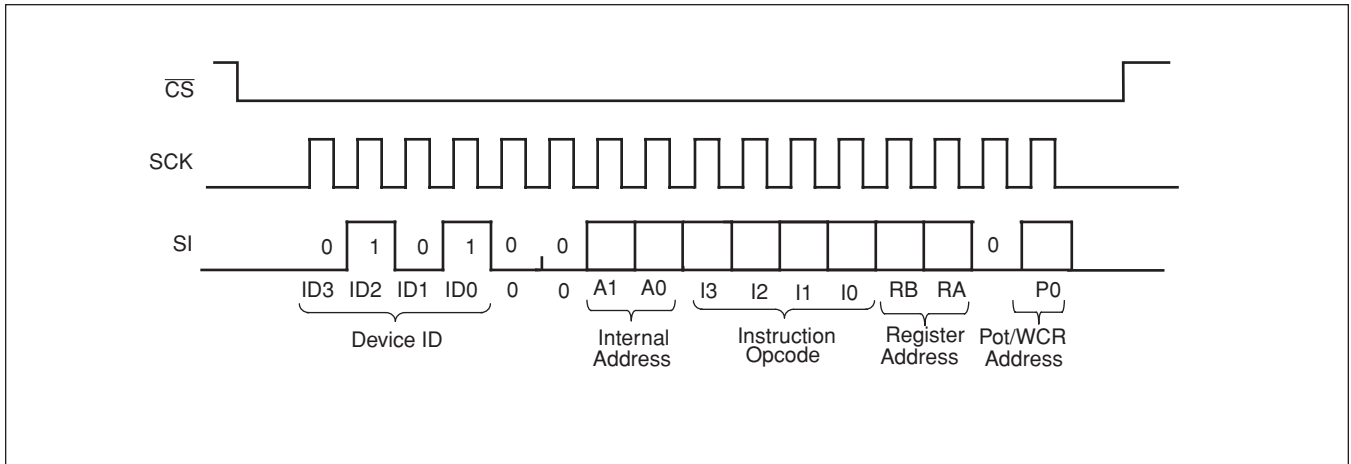


Figure 3. Three-Byte Instruction Sequence (Write)

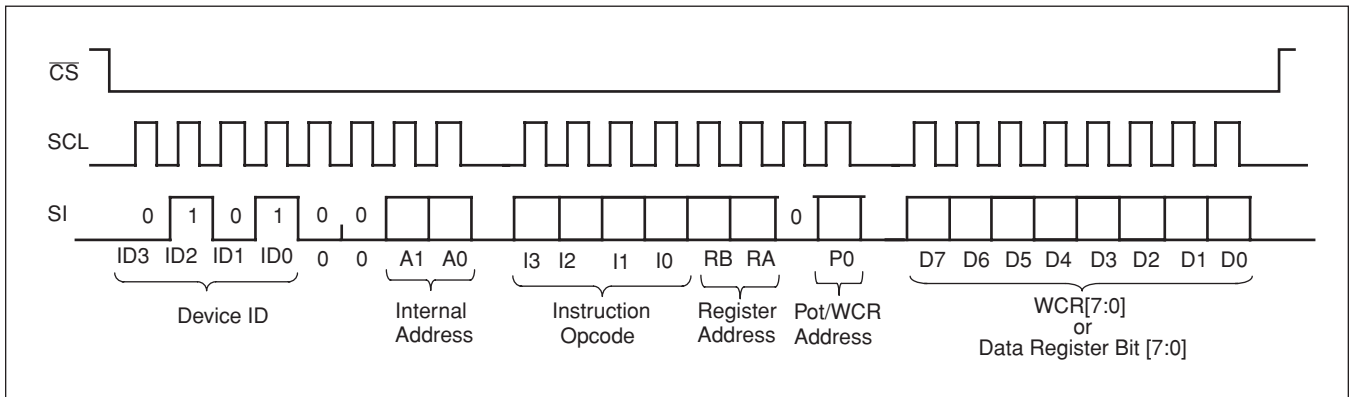


Figure 4. Three-Byte Instruction Sequence (Read)

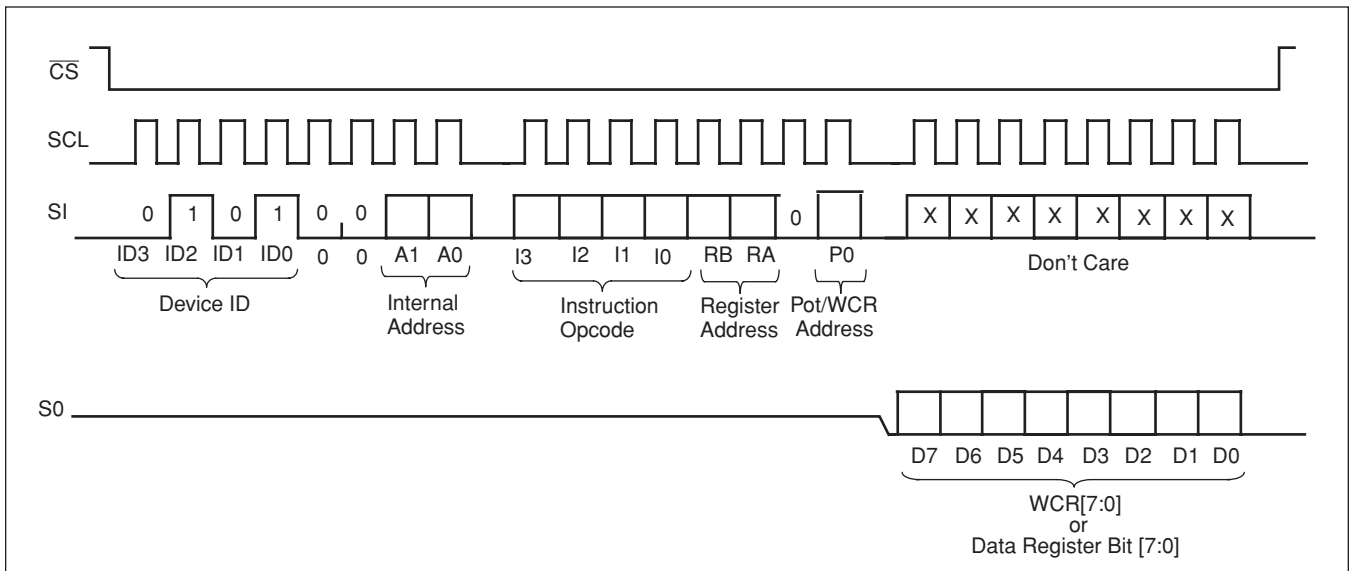


Figure 5. Three-Byte Instruction Sequence (Read Status Register)

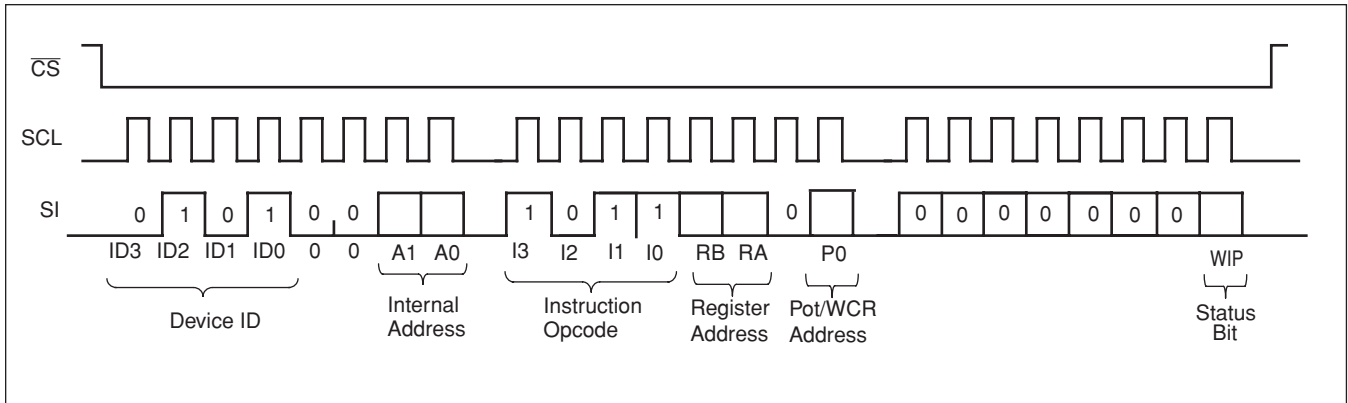


Figure 6. Increment/Decrement Instruction Sequence

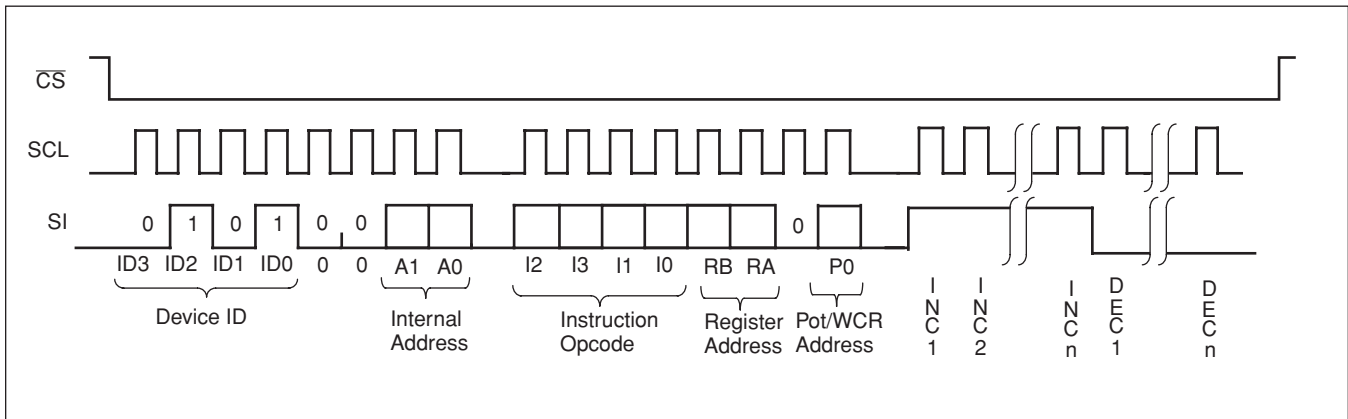
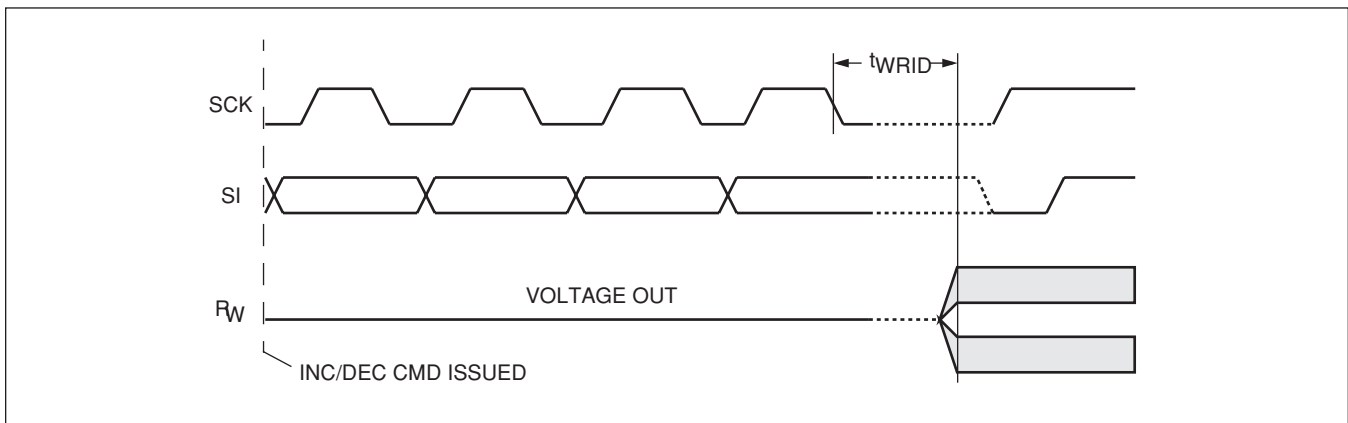


Figure 7. Increment/Decrement Timing Limits



**Table 5. Instruction Set**

Instruction	Instruction Set								Operation
	I3	I2	I1	I0	RB	RA	0	P0	
Read Wiper Counter Register	1	0	0	1	0	0	0	1/0	Read the contents of the Wiper Counter Register pointed to by P0
Write Wiper Counter Register	1	0	1	0	0	0	0	1/0	Write new value to the Wiper Counter Register pointed to by P0
Read Data Register	1	0	1	1	1/0	1/0	0	1/0	Read the contents of the Data Register pointed to by P0 and RB-RA
Write Data Register	1	1	0	0	1/0	1/0	0	1/0	Write new value to the Data Register pointed to by P0 and RB-RA
XFR Data Register to Wiper Counter Register	1	1	0	1	1/0	1/0	0	1/0	Transfer the contents of the Data Register pointed to by P0 and RB-RA to its associated Wiper Counter Register
XFR Wiper Counter Register to Data Register	1	1	1	0	1/0	1/0	0	1/0	Transfer the contents of the Wiper Counter Register pointed to by P0 to the Data Register pointed to by RB-RA
Global XFR Data Registers to Wiper Counter Registers	0	0	0	1	1/0	1/0	0	0	Transfer the contents of the Data Registers pointed to by RB-RA of all four pots to their respective Wiper Counter Registers
Global XFR Wiper Counter Registers to Data Register	1	0	0	0	1/0	1/0	0	0	Transfer the contents of both Wiper Counter Registers to their respective data Registers pointed to by RB-RA of all four pots
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	0	1/0	Enable Increment/decrement of the Control Latch pointed to by P0

**Note:** 1/0 = data is one or zero

# X9261

## INSTRUCTION FORMAT

### Read Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Wiper Position (Sent by X9261 on SO)								$\overline{CS}$ Rising Edge	
	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	0	P0	W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0		
	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	0	P0										

### Write Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Data Byte (Sent by Host on SI)								$\overline{CS}$ Rising Edge	
	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	0	P0	W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0		
	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	0	P0										

### Read Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				Data Byte (Sent by X9271 on SO)								$\overline{CS}$ Rising Edge	
	0	1	0	1	0	0	A1	A0	1	0	1	1	RB	RA	0	P0	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0		
	0	1	0	1	0	0	A1	A0	1	0	1	1	RB	RA	0	P0										

### Write Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				Data Byte (Sent by Host on SI)								$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE	
	0	1	0	1	0	0	A1	A0	1	1	0	0	RB	RA	0	P0	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0			
	0	1	0	1	0	0	A1	A0	1	1	0	0	RB	RA	0	P0											

### Global Transfer Data Register (DR) to Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR Addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	0	1	RB	RA	0	0	
	0	1	0	1	0	0	A1	A0	0	0	0	1	RB	RA	0	0	

# X9261

## Global Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR Addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	0	0	0	RB	RA	0	0		

## Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	1	0	RB	RA	0	P0		

## Transfer Data Register (DR) to Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	1	0	1	RB	RA	0	P0	

## Increment/Decrement Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Increment/Decrement (Sent by Master on SDA)				$\overline{CS}$ Rising Edge		
	0	1	0	1	0	0	A1	A0	0	0	1	0	X	X	0	P0	I/D	I/D	.	.		.	.

## Read Status Register (SR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Data Byte (Sent by X9261 on SO)								$\overline{CS}$ Rising Edge							
	0	1	0	1	0	0	A1	A0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

- Notes:** (1) "A1 ~ A0": stands for the device addresses sent by the master.  
 (2) WPx refers to wiper position data in the Counter Register  
 (2) "I": stands for the increment operation, SI held HIGH during active SCK phase (high).  
 (3) "D": stands for the decrement operation, SI held LOW during active SCK phase (high).

# X9261

## ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....-65°C to +135°C  
 Storage temperature .....-65°C to +150°C  
 Voltage on SCK any address input  
 with respect to  $V_{SS}$ .....-1V to +7V  
 $\Delta V = | (V_H - V_L) |$  ..... 5.5V  
 Lead temperature (soldering, 10 seconds).....300°C  
 $I_W$  (10 seconds) .....  $\pm 6$ mA

## COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

Device	Supply Voltage ( $V_{CC}$ ) <sup>(4)</sup> Limits
X9261	5V $\pm 10\%$
X9261-2.7	2.7V to 5.5V

## POTENTIOMETER CHARACTERISTICS (Over recommended industrial operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
$R_{TOTAL}$	End to End Resistance		100		k $\Omega$	T version
$R_{TOTAL}$	End to End Resistance		50		k $\Omega$	U version
	End to End Resistance Tolerance			$\pm 20$	%	
	Power Rating			50	mW	25°C, each pot
$I_W$	Wiper Current			$\pm 3$	mA	
$R_W$	Wiper Resistance			300	$\Omega$	$I_W = \pm 3$ mA @ $V_+ = 3$ V
$R_W$	Wiper Resistance			150	$\Omega$	$I_W = \pm 3$ mA @ $V_+ = 5$ V
$V_{TERM}$	Voltage on any $R_H$ or $R_L$ Pin	$V_{SS}$		$V_{CC}$	V	$V_{SS} = 0$ V
	Noise		-120		dBV	Ref: 1V
	Resolution		0.4		%	
	Absolute Linearity <sup>(1)</sup>			$\pm 1$	MI <sup>(3)</sup>	$R_{W(n)(actual)} - R_{W(n)(expected)}$ <sup>(5)</sup>
	Relative Linearity <sup>(2)</sup>			$\pm 0.6$	MI <sup>(3)</sup>	$R_{W(n+1)} - [R_{W(n)} + MI]$ <sup>(5)</sup>
	Temperature Coefficient of $R_{TOTAL}$		$\pm 300$		ppm/°C	
	Ratiometric Temp. Coefficient			20	ppm/°C	
$C_H/C_L/C_W$	Potentiometer Capacitances		10/10/25		pF	See Macro model
$I_{al}$	$R_W, R_H, R_L$ Leakage		0.1	10.0	$\mu$ A	Device in stand by. $V_{in} = V_{SS}$ to $V_{CC}$

- Notes:** (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.  
 (2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.  
 (3)  $MI = RTOT / 255$  or  $(R_H - R_L) / 255$ , single pot  
 (4) During power up  $V_{CC} > V_H, V_L$ , and  $V_W$ .  
 (5)  $n = 0, 1, 2, \dots, 255$ ;  $m = 0, 1, 2, \dots, 254$ .

# X9261

## D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> supply current (active)			400	μA	f <sub>SCK</sub> = 2.5 MHz, SO = Open, V <sub>CC</sub> =6V Other Inputs = V <sub>SS</sub>
I <sub>CC2</sub>	V <sub>CC</sub> supply current (nonvolatile write)		1	5	mA	f <sub>SCK</sub> = 2.5MHz, SO = Open, V <sub>CC</sub> =6V Other Inputs = V <sub>SS</sub>
I <sub>SB</sub>	V <sub>CC</sub> current (standby)			5	μA	SCK = SI = V <sub>SS</sub> , Addr. = V <sub>SS</sub> , $\overline{CS}$ = V <sub>CC</sub> = 6V
I <sub>LI</sub>	Input leakage current			10	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>LO</sub>	Output leakage current			10	μA	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>
V <sub>IH</sub>	Input HIGH voltage	V <sub>CC</sub> × 0.7		V <sub>CC</sub> + 1	V	
V <sub>IL</sub>	Input LOW voltage	-1		V <sub>CC</sub> × 0.3	V	
V <sub>OL</sub>	Output LOW voltage			0.4	V	I <sub>OL</sub> = 3mA
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> - 0.8			V	I <sub>OH</sub> = -1mA, V <sub>CC</sub> ≥ +3V
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> - 0.4			V	I <sub>OH</sub> = -0.4mA, V <sub>CC</sub> ≤ +3V

## ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	years

## CAPACITANCE

Symbol	Test	Max.	Units	Test Conditions
C <sub>OUT</sub> <sup>(6)</sup>	Output capacitance (SO)	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> <sup>(6)</sup>	Input capacitance (A0, A1, SI, $\overline{CS}$ , $\overline{WP}$ , $\overline{HOLD}$ , and SCK)	6	pF	V <sub>IN</sub> = 0V

## POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t <sub>r</sub> V <sub>CC</sub> <sup>(6)</sup>	V <sub>CC</sub> Power-up rate	0.2	50	V/ms
t <sub>PUR</sub> <sup>(7)</sup>	Power-up to initiation of read operation		1	ms

## POWER UP AND DOWN REQUIREMENTS

There are no restrictions on the power-up or power-down conditions of V<sub>CC</sub> and the voltages applied to the potentiometer pins provided that V<sub>CC</sub> is always more positive than or equal to V<sub>H</sub>, V<sub>L</sub>, and V<sub>W</sub>, i.e., V<sub>CC</sub> ≥ V<sub>H</sub>, V<sub>L</sub>, V<sub>W</sub>. The V<sub>CC</sub> power-up timing spec is always in effect.

## A.C. TEST CONDITIONS

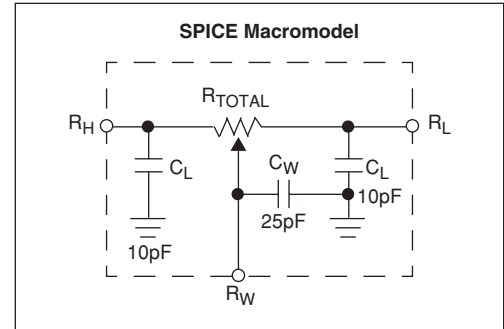
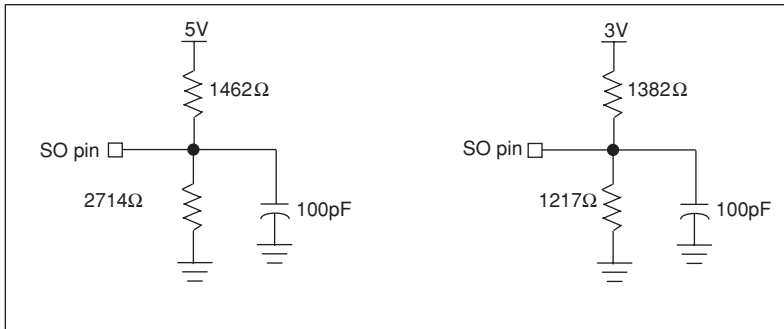
Input Pulse Levels	V <sub>CC</sub> × 0.1 to V <sub>CC</sub> × 0.9
Input rise and fall times	10ns
Input and output timing level	V <sub>CC</sub> × 0.5

**Notes:** (6) This parameter is not 100% tested

(7) t<sub>PUR</sub> and t<sub>PJW</sub> are the delays required from the time the (last) power supply (V<sub>CC</sub>-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

# X9261

## EQUIVALENT A.C. LOAD CIRCUIT



## AC TIMING

Symbol	Parameter	Min.	Max.	Units
$f_{SCK}$	SSI/SPI clock frequency		2	MHz
$t_{CYC}$	SSI/SPI clock cycle time	500		ns
$t_{WH}$	SSI/SPI clock high time	200		ns
$t_{WL}$	SSI/SPI clock low time	200		ns
$t_{LEAD}$	Lead time	250		ns
$t_{LAG}$	Lag time	250		ns
$t_{SU}$	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input setup time	50		ns
$t_H$	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input hold time	50		ns
$t_{RI}$	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input rise time		2	$\mu$ s
$t_{FI}$	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input fall time		2	$\mu$ s
$t_{DIS}$	SO output disable time	0	250	ns
$t_V$	SO output valid time		200	ns
$t_{HO}$	SO output hold time	0		ns
$t_{RO}$	SO output rise time		100	ns
$t_{FO}$	SO output fall time		100	ns
$t_{HOLD}$	$\overline{HOLD}$ time	400		ns
$t_{HSU}$	$\overline{HOLD}$ setup time	100		ns
$t_{HH}$	$\overline{HOLD}$ hold time	100		ns
$t_{HZ}$	$\overline{HOLD}$ low to output in high Z		100	ns
$t_{LZ}$	$\overline{HOLD}$ high to output in low Z		100	ns
$T_I$	Noise suppression time constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ inputs		10	ns
$t_{CS}$	$\overline{CS}$ deselect time	2		$\mu$ s
$t_{WPASU}$	$\overline{WP}$ , A0, A1 setup time	0		ns
$t_{WPAH}$	$\overline{WP}$ , A0, A1 hold time	0		ns



# X9261

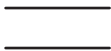


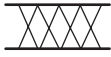

## HIGH-VOLTAGE WRITE CYCLE TIMING

Symbol	Parameter	Typ.	Max.	Units
$t_{WR}$	High-voltage write cycle time (store instructions)	5	10	ms

## XDCP TIMING

Symbol	Parameter	Min.	Max.	Units
$t_{WRPO}$	Wiper response time after the third (last) power supply is stable	5	10	$\mu$ s
$t_{WRL}$	Wiper response time after instruction issued (all load instructions)	5	10	$\mu$ s

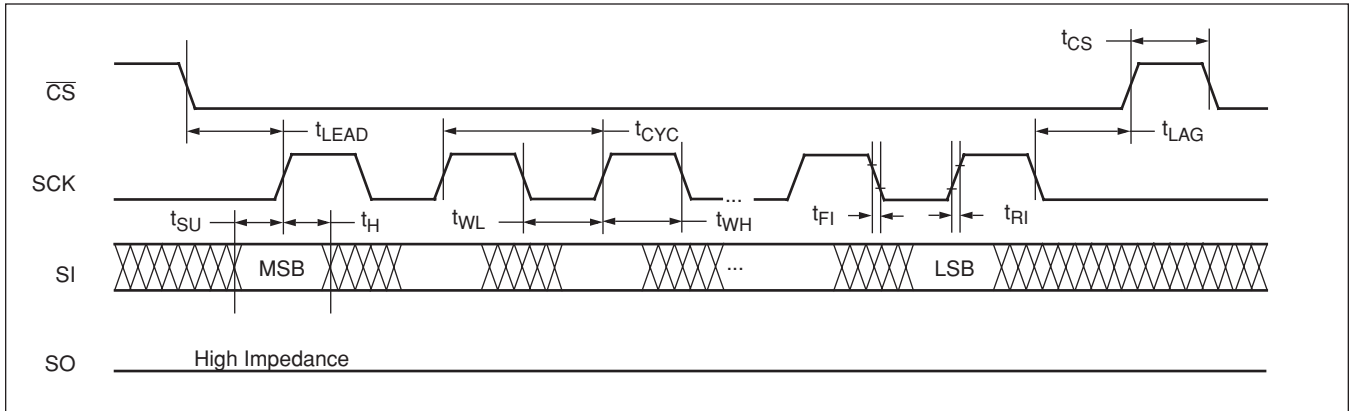
## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

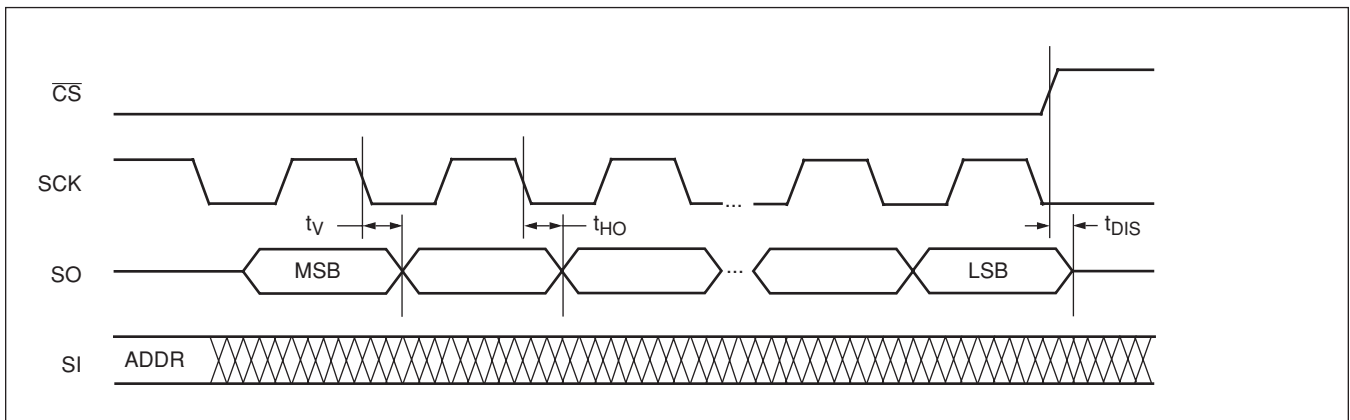
# X9261

## TIMING DIAGRAMS

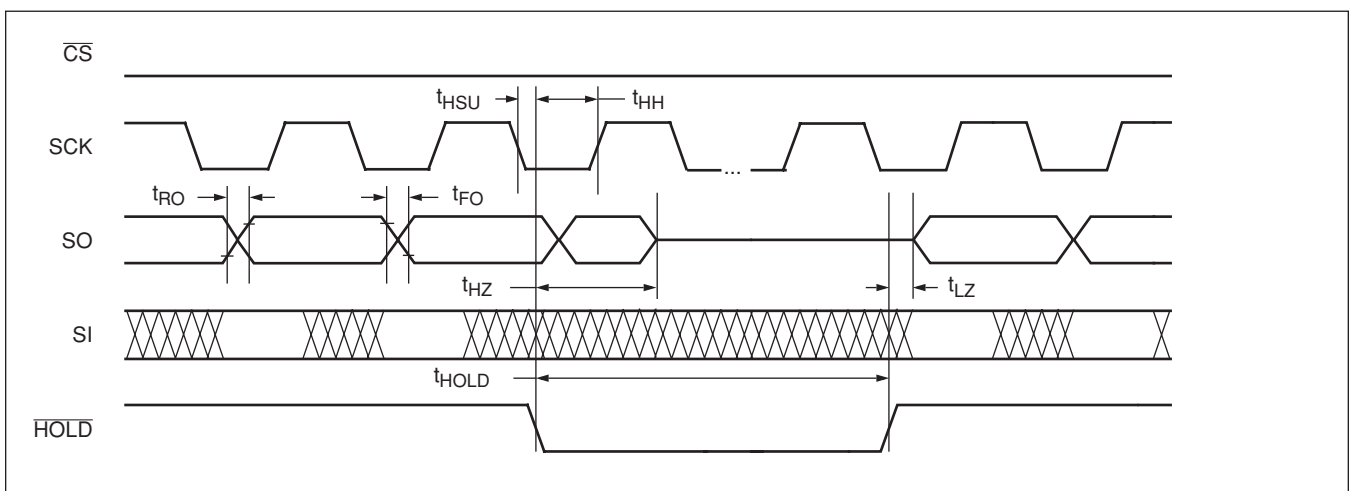
### Input Timing



### Output Timing

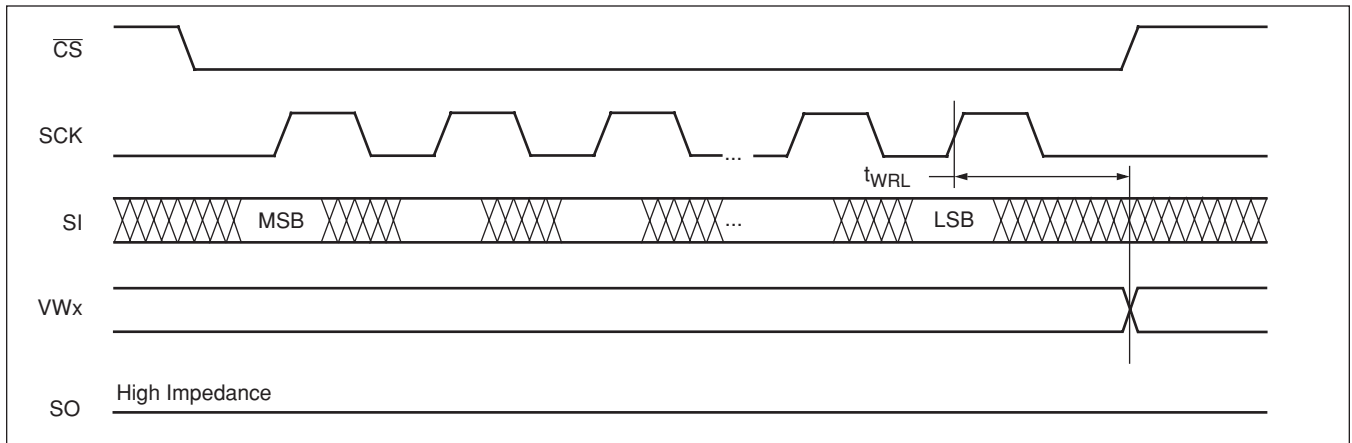


### Hold Timing

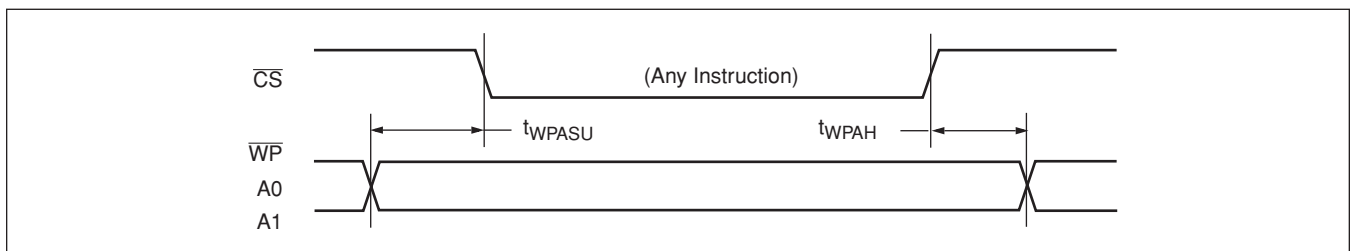


# X9261

## XDCP Timing (for All Load Instructions)

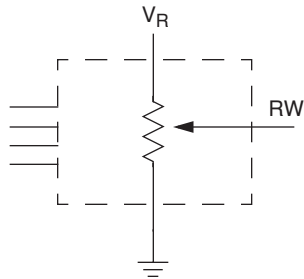


## Write Protect and Device Address Pins Timing

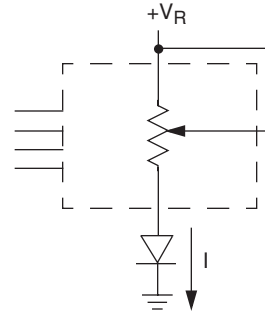


## APPLICATIONS INFORMATION

### Basic Configurations of Electronic Potentiometers



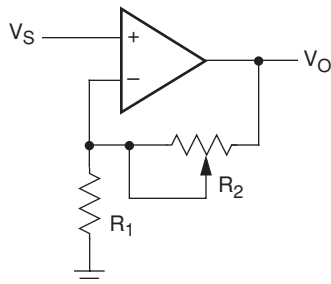
Three terminal Potentiometer;  
Variable voltage divider



Two terminal Variable Resistor;  
Variable current

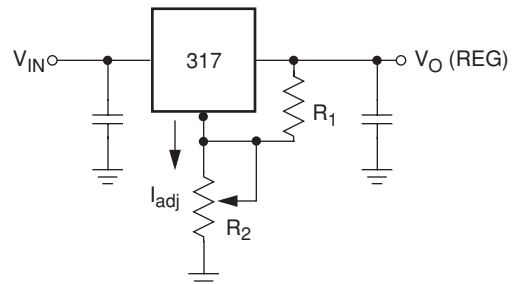
### Application Circuits

#### Noninverting Amplifier



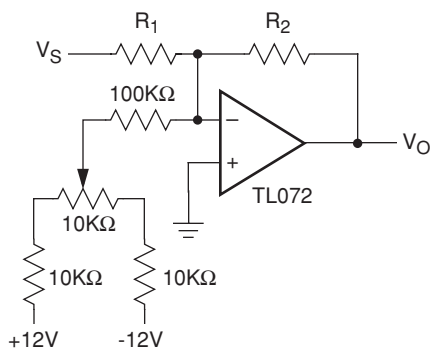
$$V_O = (1 + R_2/R_1) V_S$$

#### Voltage Regulator

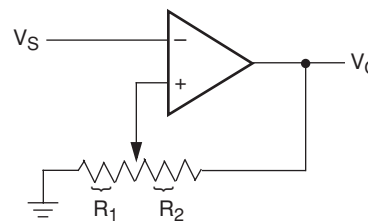


$$V_O (\text{REG}) = 1.25V (1 + R_2/R_1) + I_{\text{adj}} R_2$$

#### Offset Voltage Adjustment



#### Comparator with Hysteresis

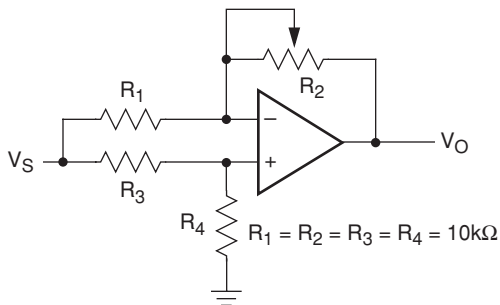


$$V_{UL} = \{R_1 / (R_1 + R_2)\} V_O (\text{max})$$

$$V_{LL} = \{R_1 / (R_1 + R_2)\} V_O (\text{min})$$

Application Circuits (continued)

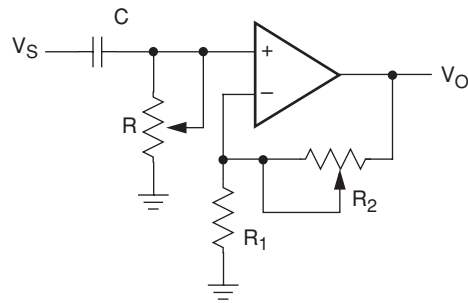
Attenuator



$$V_O = G V_S$$

$$-1/2 \leq G \leq +1/2$$

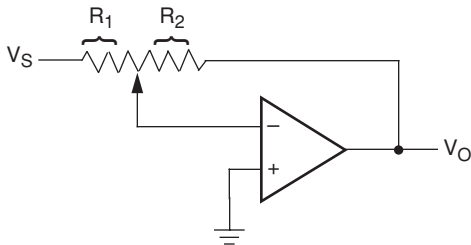
Filter



$$G_O = 1 + R_2/R_1$$

$$f_c = 1/(2\pi RC)$$

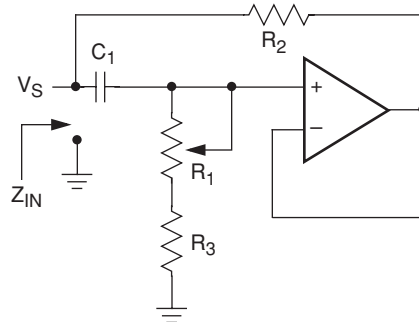
Inverting Amplifier



$$V_O = G V_S$$

$$G = -R_2/R_1$$

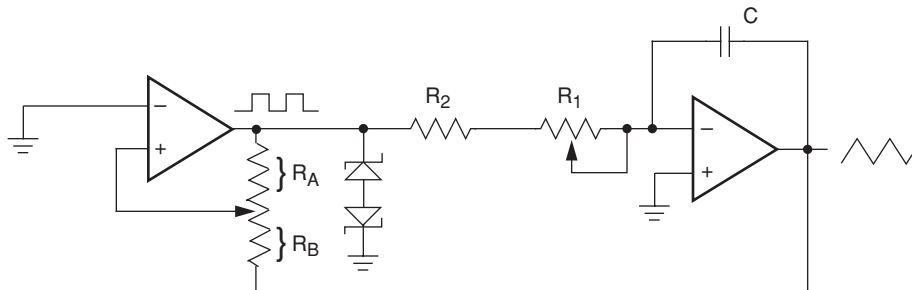
Equivalent L-R Circuit



$$Z_{IN} = R_2 + s R_2 (R_1 + R_3) C_1 = R_2 + s L_{eq}$$

$$(R_1 + R_3) \gg R_2$$

Function Generator



$$\text{frequency} \propto R_1, R_2, C$$

$$\text{amplitude} \propto R_A, R_B$$

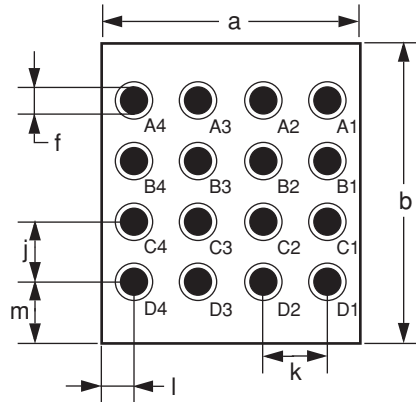
# X9261

## PACKAGING INFORMATION

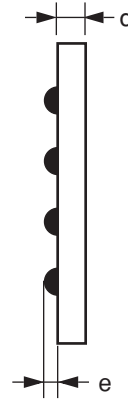
### 16-Bump Chip Scale Package (CSP B16) Package Outline Drawing



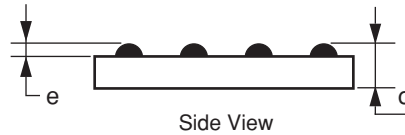
Top View (Marking Side)



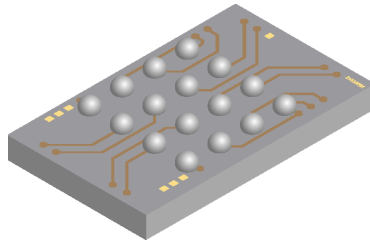
Bottom View (Bumped Side)



Side View



Side View



### Package Dimensions

	Symbol	Millimeters			Inches		
		Min	Nominal	Max	Min	Nominal	Max
Package Width	a	2.745	2.775	2.805			
Package Length	b	4.523	4.553	4.583			
Package Height	c	0.644	0.677	0.710			
Body Thickness	d	0.444	0.457	0.470			
Ball Height	e	0.200	0.220	0.240			
Ball Diameter	f	0.300	0.320	0.340			
Ball Pitch – Width	j		0.65				
Ball Pitch – Length	k		0.65				
Ball to Edge Spacing – Width	l	0.388	0.413	0.438			
Ball to Edge Spacing – Length	m	1.277	1.302	1.327			

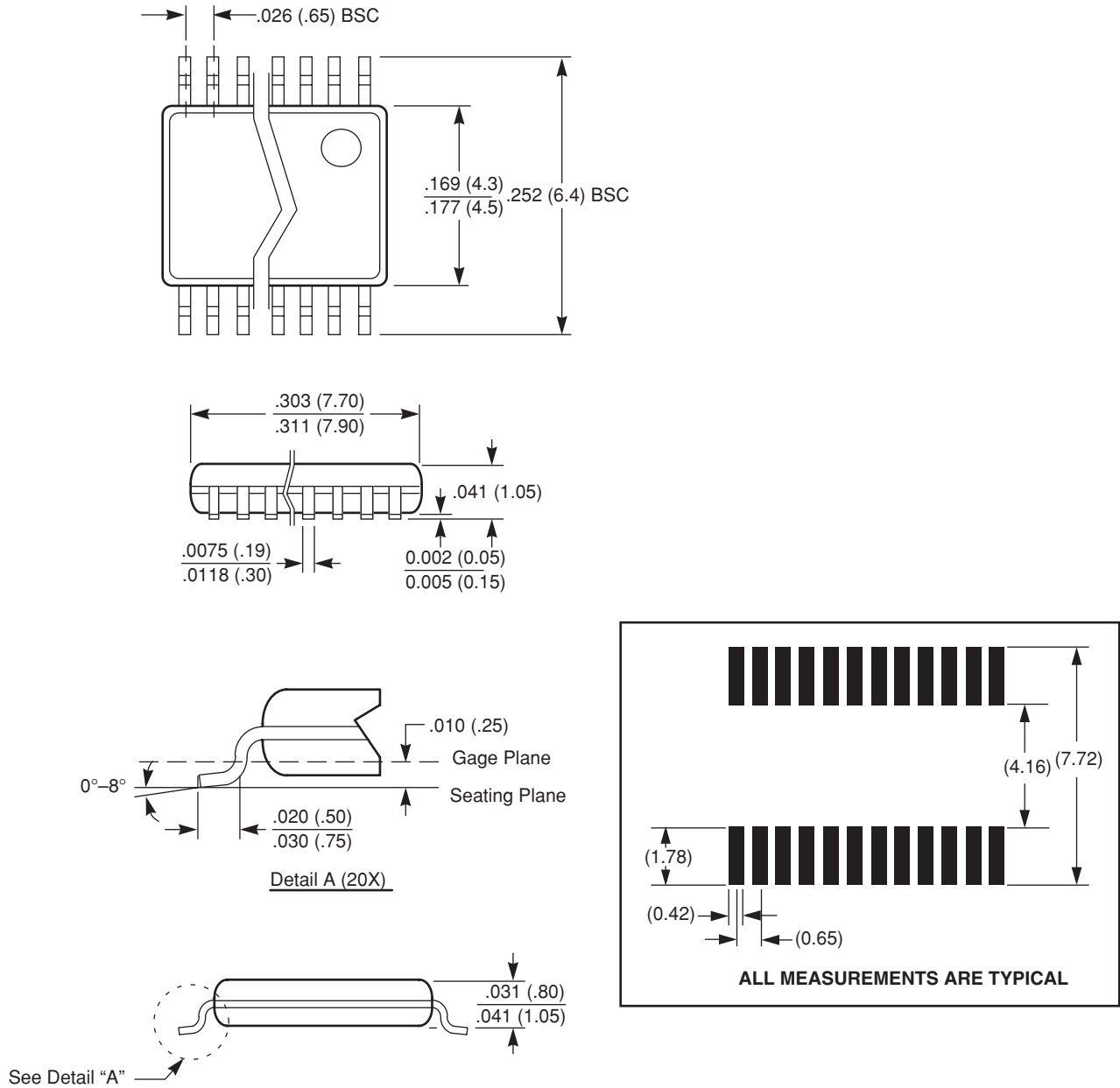
### Ball Matrix:

	4	3	2	1
A	R <sub>H1</sub>	A1	$\overline{\text{CS}}$	R <sub>H0</sub>
B	R <sub>L1</sub>	SI	WP	R <sub>W0</sub>
C	R <sub>W1</sub>	HOLD	SO	R <sub>L0</sub>
D	V <sub>SS</sub>	SCK	A0	V <sub>CC</sub>

# X9261

## PACKAGING INFORMATION

### 24-Lead Plastic, TSSOP, Package Code V24

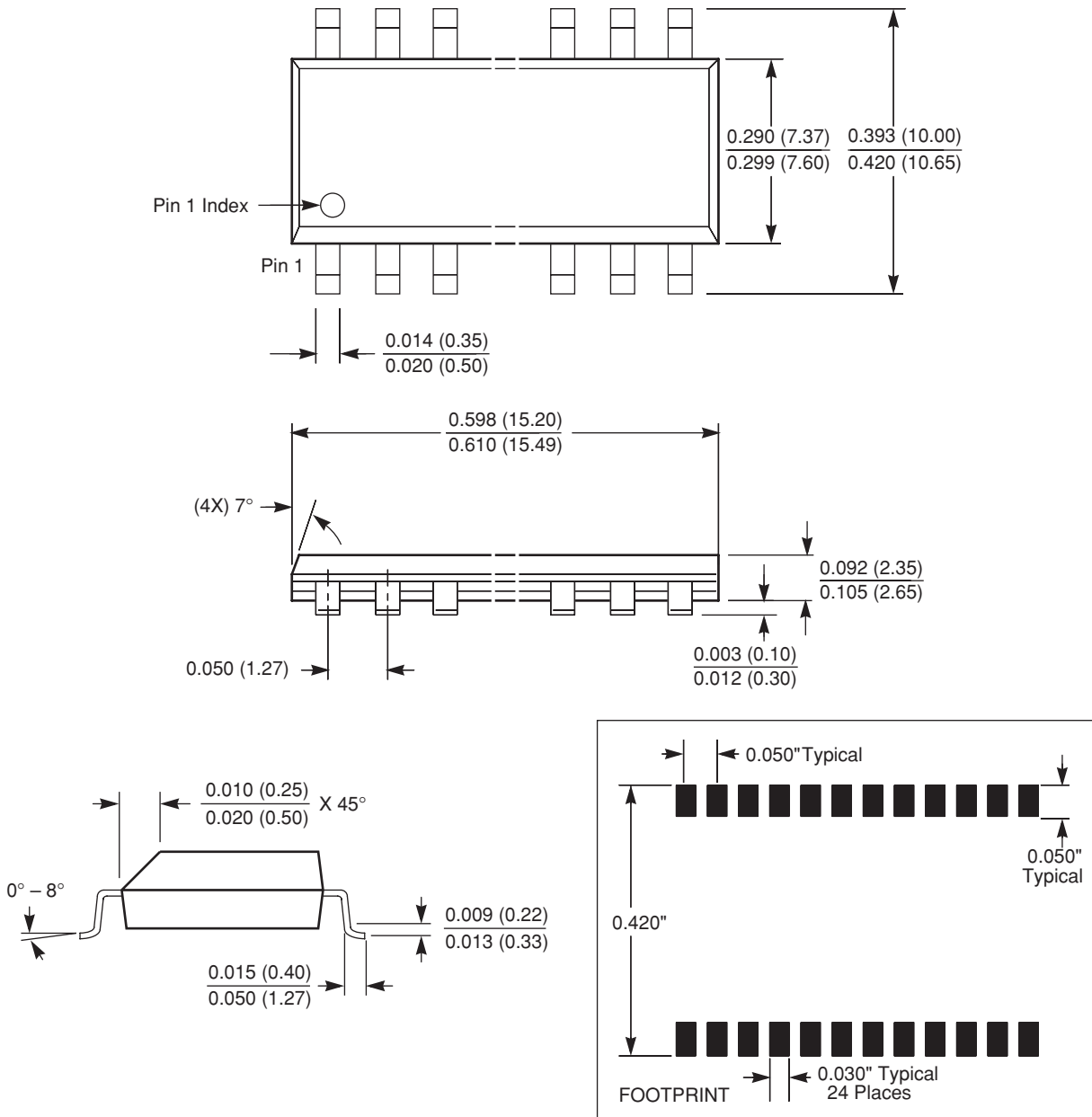


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

# X9261

## PACKAGING INFORMATION

### 24-Lead Plastic Small Outline Gull Wing Package Type S

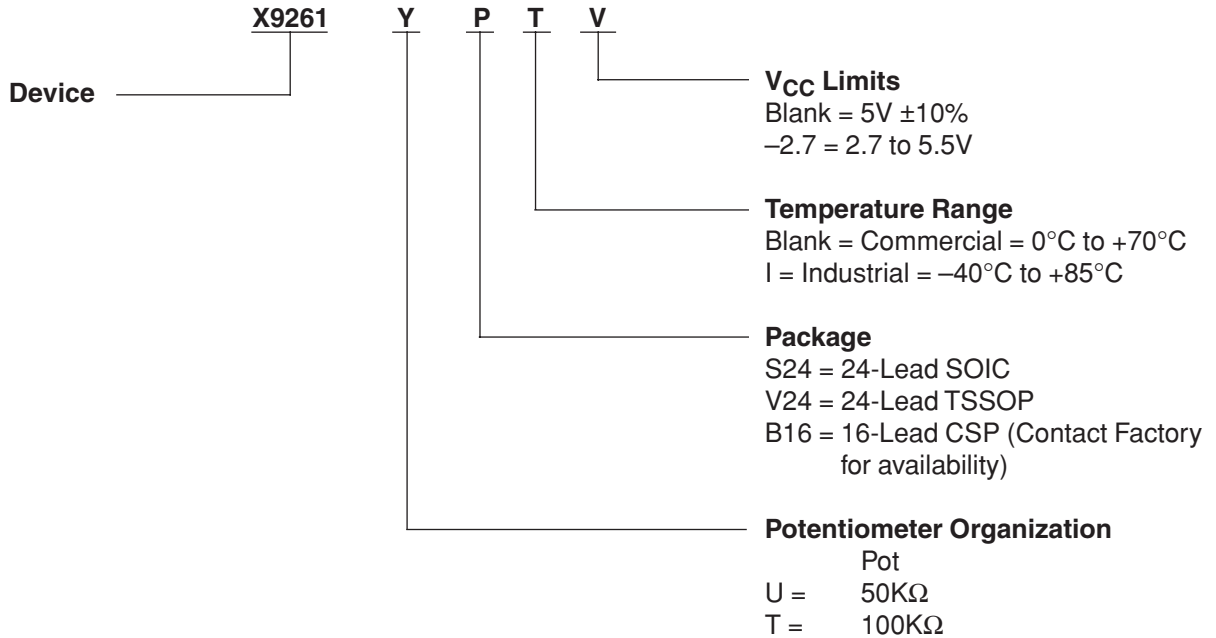


**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**



# X9261

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.